SPLIT MULTIPLIER ARRAY AND METHOD OF OPERATION

ABSTRACT OF THE DISCLOSURE

There is disclosed a multiplier circuit for use in a data processor. The multiplier circuit comprises a partial products generating circuit that receives a multiplicand value and a multiplier value and generates a group of partial products. The multiplier circuit also comprises a split array for adding the partial products. A first summation array comprises a first group of adders that sum the even partial products to produce an even summation value. A second summation array comprises a second group of adders that sum the odd partial products to produce an odd summation value. The even and odd summation values are then summed to produce the output of the multiplier.